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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/577,980	05/25/2000	Jun Yoshida	35.C14505	6464

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FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/577,980	YOSHIDA ET AL.	
	Examiner	Art Unit	
	Guy J. Lamarre, P.E.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 5-10, 21, 25-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-10,21 and 25-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 May 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL OFFICE ACTION

0. This office action is in response to Applicants' Amendment of *7/29/2004*. The Examiner has considered the IDS jointly filed.

0.1 **Claims 1, 5-10, 21, 25-30** are amended, **Claims 2-4, 11-20, 22-24, 31-40** are cancelled. **Claims 1, 5-10, 21, 25-30** remain pending.

0.2 The objections and rejections under 35 U.S.C. 101 & 112 of record are withdrawn in response to Applicants' Amendments.

0.2.1 The prior art rejections of record are maintained in response to Applicants' Amendments.

Response to Arguments

1. Applicants' arguments have been fully considered, but are not persuasive.

REMARKS

2. In response to **Claims 1, 5-10, 21, 25-30,** Applicants argue, on page 8 et seq., that the prior art of record does not teach the claims as amended.

Examiner disagrees and notes that **Ott**, in Fig. 1, discloses the claimed parallel coding structure wherein a communication processor receives an original input sequence, feeds such input sequence into plural parallel *identical or different coders*, such as CRC/RS/ARQ codes, either separated or concatenated in series with other coding means.

Examiner also notes that **Kobayashi et al.**, in Fig. 1, discloses the claimed algorithm switching means to select one ECC codec algorithm out of plural encoding/decoding algorithms based on computation needs of a user at col. 4 line 30 et seq. and Figs. 1-14, such encoding/decoding algorithms comprising '*a variety of ECC, such as turbo/convolutional/RLL/CRC/RS codes,*' in col. 3 line 36.

Examiner further notes that **Kobayashi et al.** defines two 1st and 2nd coders receiving equal inputs with the second coder having inputs thereto interleaved, both 1st and 2nd coders concurrently operating as a turbo coder. Thus the claimed invention reads on such turbo coder.

Examiner maintains that **Kobayashi's** turbo coder incorporated into the parallel structure of **Ott's** Fig. 1: blocks 102-104 renders obvious the claimed invention.

Claim Objections

3. **Claims 1, 5-10, 21, 25-30** are objected to for reciting '*interleaving means*' instead of ''*interleaving unit*' in Claim 1, and '*adapted to*' in passim in **Claims 1, 5-10, 21, 25-30**. It has been held that the recitation that an element is "adapted to" perform a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138.

Appropriate correction is required.

Claim Rejections - 35 USC ' 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4.1 **Claims 1, 5-10, 21, 25-30** are rejected under 35 U.S.C. 102 (e) as being anticipated by **Kobayashi et al.** (US Patent No. 6,029,264; April 28, 1997).

As per Claims 1, 5-10, 21, 25-30, Kobayashi et al. discloses algorithm means to select from a plurality of encoding/decoding algorithms based on computation needs of a user at col. 4 line 30 et seq., e.g., in Fig. 12C below an equivalent turbo/convolutional/concatenated/parallel concatenated system comprising: maximum likelihood decoder, 1st error detector/corrector, a

code demodulator, and a second error detector/corrector, digital modulation means, code or block dividing or partitioning (Fig. 5), permutation or interleaving for burst error reduction; means for post coder for partial response in col. 2 line 21; means for cyclically coded bit in col. 6 line 40; means for detecting and correcting errors based on predetermined parameters such as number of errors, e.g., "*if the received sequence does not satisfy parity-check equations, then the receiver detects the existence of some errors and, in some cases, can correct them.*" in col. 1 lines 39-et seq.;

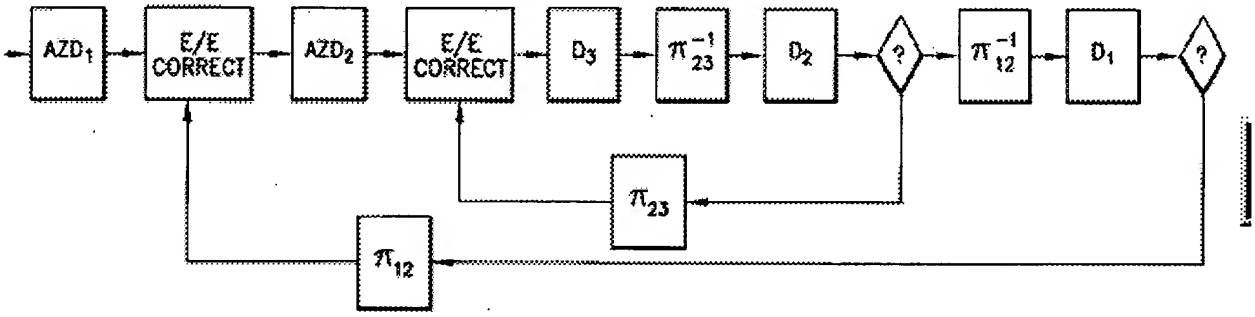


FIG.12C

means for run-length limiting coding, e.g., "*digital recording, is run-length limited codes, denoted (d,k)-limited codes. The integer parameters d and k represent the minimum and maximum numbers of runs of either 0's or 1's that are allowed in the encoded sequence. The lower bound d is chosen from the ISI consideration, and the upper bound k is set to insure clock synchronization capability at the receiver side,*" in col. 2 lines 39-46; and for means for cyclically coding bits in col. 6 line 40.

4.2 Claims 1, 5-10, 21, 25-30 are rejected under 35 U.S.C. 102(e) as being anticipated by **Ott** (US Patent No. 6,182,264; May 22, 1998).

As per Claims 1, 5-10, 21, 25-30, Ott teaches an equivalent routine in col. 1 line 5 – col. 11 line 64 wherein a processor, in e.g., Fig. 1: Block 117, is configured to dynamically select one of plural error correction processes/techniques based on measured transmission channel error

rates or channel conditions so as to reduce power consumption or circuit hardware or both, e.g., when error rate is in a low or high state such that power consumed while processing one of plural error correction codes corresponds to an appropriate error rate as depicted by Figs. 1-4; means for concurrent coder operation under algorithmic control, e.g., **EDC** in e.g., Fig. 1: Block 117.

Ott discloses means for controlling power consumption in an electronic device, said device including a data receiver (Fig. 1: block 101), a data transmitter (Fig. 1: block 118), and means for performing a plurality of error detection and/or correction techniques said method comprising: receiving data having a given EDC coding;

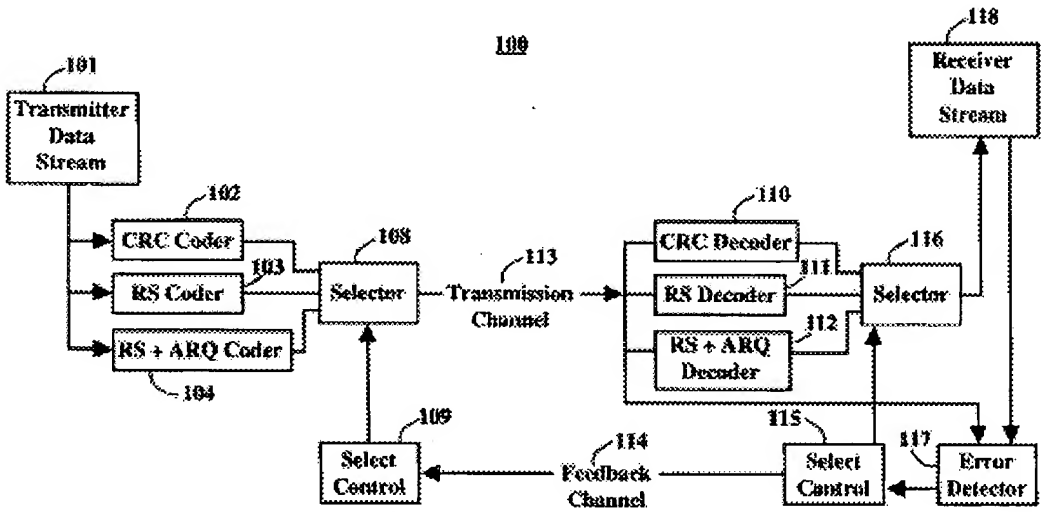


FIG. 1

determining an error rate (Fig. 4: block 401) corresponding to said received data, said error rate being determined by an initial one of said plurality of error detection and/or correction techniques; comparing said error rate to at least one error threshold value; and selecting (Fig. 4: block selects 408 and 404) one of said plurality of error detection and/or correction techniques of said electronic device based on an outcome of said comparing step (Fig. 4: block compares 407 and 402-403); determining an error rate (Fig. 4: block decision 401) corresponding to said

received data, said error rate being determined by an initial one of said plurality of error detection and/or correction techniques (Fig. 4: block selects 408 and 404). Examiner notes that it is clear to those of ordinary skill in data communications that error detection generally requires less hardware that error correction and that less energy is consumed/required for error detection processing than for error correction because less signal processing is performed in detection.

Ott also discloses procedure wherein error threshold value corresponds to an error rate which will ensure that said selected error detection and/or correction technique is one which consumes a lowest amount of power while maintaining a desired signal-to noise ratio in Fig. 4;

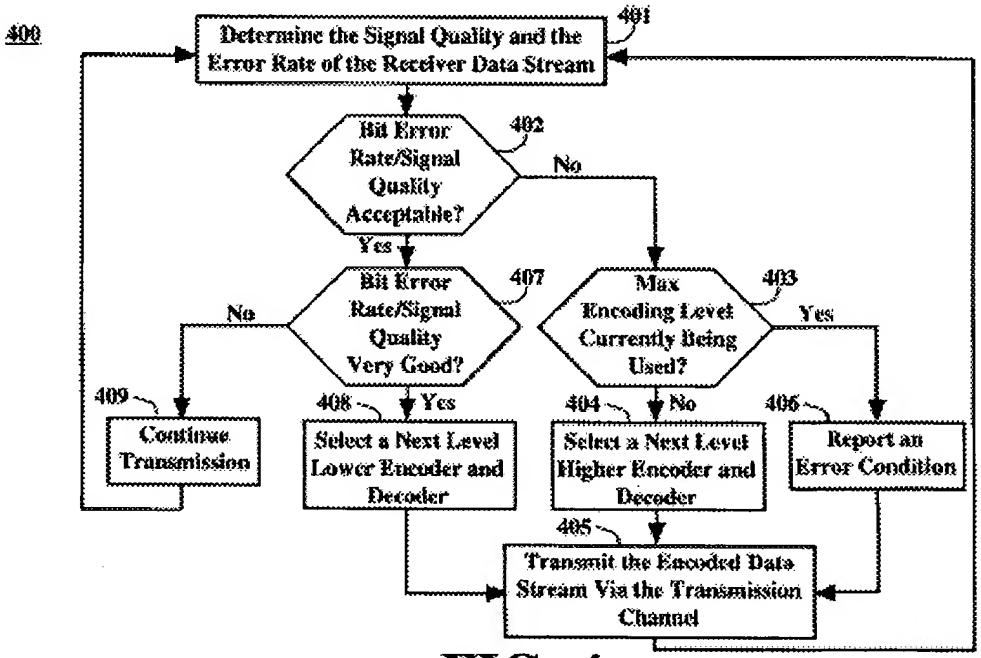


FIG. 4

wherein if said error rate is below said error threshold value, said selecting step includes: selecting an error detection and/or correction technique which is less complex and consumes less power than said initial error detection and/or correction circuit **in Fig. 4**.; wherein if said error rate exceeds said error threshold value, said selecting step includes: selecting an error detection and/or correction technique which is more complex and consumes more power than said initial

error detection and/or correction circuit **in Fig. 4; and** further comprising: means for adjusting at least one controller operating parameter to support performance of said selected error detection and/or correction technique **in Fig. 4; and** further comprising: adjusting an output signal level of said data transmitter in accordance with an outcome of said comparing step **in Fig. 4**; and whereby a user or a controller provides an external signal or signal to enable selection of error detection and/or correction technique in accordance with said external signal or signal, said operation being used for power level compensation **in Fig. 4**.; wherein said external signal causes an error detection and/or correction technique having a higher complexity and power consumption level than said initial error detection and/or correct technique, said external signal thereby improving signal-to-noise ratio at an expense of increased power consumption **in Fig. 4**; and wherein said external signal causes an error detection and/or correction technique having a lower complexity and power consumption level than said initial error detection and/or correct technique, said external signal thereby improving power consumption at an expense of a lower signal-to-noise ratio **in Fig. 4;** and wherein said plurality of error detection and/or correction techniques is at least three, and wherein said comparing step includes: comparing said error rate to a first error threshold value, and if said error rate is less than said first error rate, selecting an error detection and/or correction technique of low complexity and power consumption requirements; if said error rate is greater than said first error rate but lower than a second error threshold value, selecting an error detection and/or correct technique of medium complexity and power consumption requirements; and if said error rate is greater than said second error threshold value, selecting an error detection and/or correction technique of high complexity and power consumption requirements **in Fig. 4**.

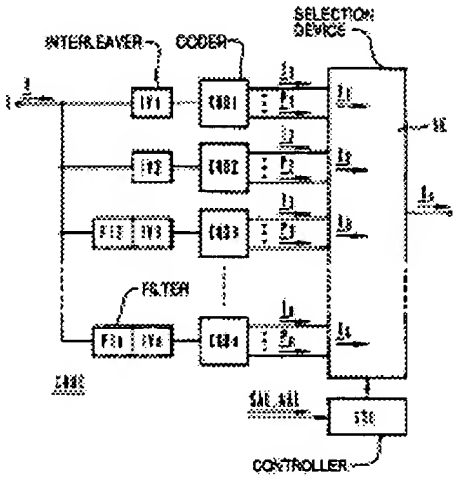
Ott further discloses, in Figs. 1 and 4, an algorithm for controlling power consumption in an electronic device, said device including a data receiver (Fig. 1), a data transmitter (Fig. 1), and

means for performing a plurality of error detection and/or correction techniques (Fig. 1: blocks 102-104 and 110-112), said method comprising: receiving an external or manually or automatically entered signal from a user; and selecting one of a plurality of error detection and/or correction techniques in accordance with said external signal, said plurality of error detection and/or correction techniques consuming different levels of power and having different levels of complexity; wherein said external signal causes an error detection and/or correction technique which is one of the following: an error detection and/or correction technique (cols. 4-5: **crc or rs or turbo or convolutional coding, etc**) having a higher complexity and power consumption level than a currently selected error detection and/or correct technique, said external signal thereby improving signal-to-noise ratio at an expense of increased power consumption; and an error detection and/or correction technique having a lower complexity and power consumption level than said currently selected error detection and/or correct technique, said external signal thereby improving power consumption at an expense of a lower signal-to-noise ratio **and** whereby a user or a controller provides an external signal or signal to enable selection of error detection and/or correction technique in accordance with said external signal or signal, said operation being used for power level compensation **in Fig. 4**.

4.3 Claims 1, 5-10, 21, 25-30 are rejected under 35 U.S.C. 102(b) as being anticipated by **Hagenauer et al.** (US Patent No. 5,729,560; 17 Mar. 1998) of IDS filed *7/29/2004*.

As per Claims 1, 5-10, 21, 25-30, Hagenauer et al. teaches an equivalent routine, in col. 1 line 5 et seq., wherein a communication processor receives an original input sequence, feeds such input sequence into a parallel coding structure comprising plural '*identical or different coders*', such as turbo codes, in series with interleaving means to combat debilitating channel distances as depicted in, e.g., Fig. 1 below and described in col. 3 lines 14-21 et seq. Inverse

operations to recover the original sequence via decoding and deinterleaving means are shown in Fig. 2.



4.4 **Claims 1, 5-10, 21, 25-30** are rejected under 35 U.S.C. 102(e) as being anticipated by **Park** (EP 0 998 789 A; 14 Oct. 1999) of IDS filed *7/29/2004*.

As per Claims 1, 5-10, 21, 25-30, Figs. 1-5 & description thereoff depict an equivalent structure.

Claim Rejections - 35 USC § 103

5. **Claims** 1, 5-10, 21, 25-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ott** (US Patent No. 6,182,264; May 22, 1998) in view of **Kobayashi** (US Patent No. 6,029,264; 28 Apr. 1997).

As per Claims 1, 5-10, 21, 25-30, Ott substantially discloses data processing means, in col. 1 line 5 – col. 11 line 64, wherein a processor is configured to dynamically select one of plural error correction processes/techniques/algorithms based on measured transmission channel error rates or channel conditions so as to reduce power consumption or circuit hardware or both, e.g., when error rate is in a low or high state such that power consumed while processing one of plural error correction codes corresponds to an appropriate error rate as depicted by Figs. 1-4.

Ott also discloses means for controlling power consumption in an electronic device, said device including a data receiver (Fig. 1: block 101), a data transmitter (Fig. 1: block 118), and means for performing a plurality of error detection and/or correction techniques said method comprising: receiving data having a given EDC coding; means for concurrent coder operation under algorithmic control, e.g., **EDC** in e.g., Fig. 1: Block 117

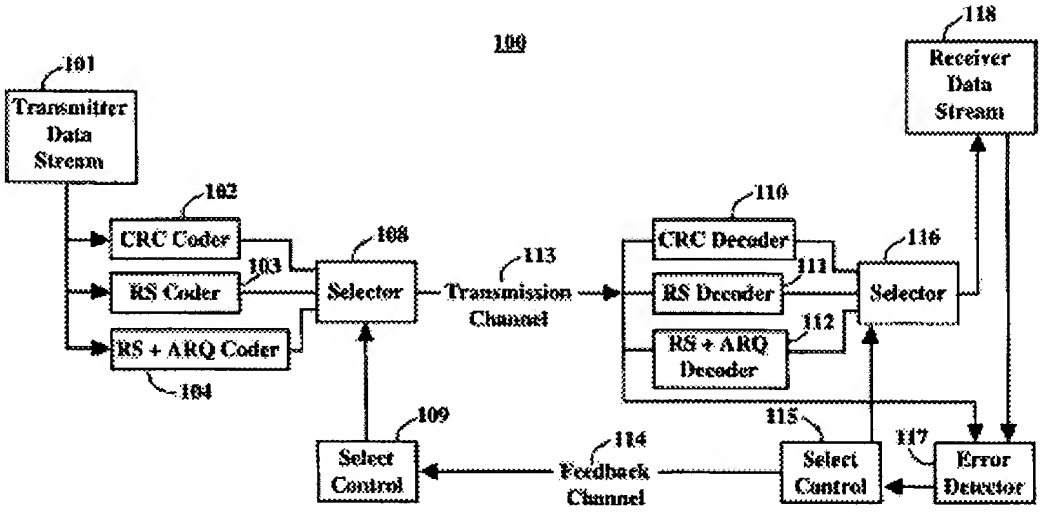


FIG. 1

determining an error rate (Fig. 4: block 401) corresponding to said received data, said error rate being determined by an initial one of said plurality of error detection and/or correction techniques; comparing said error rate to at least one error threshold value; and **selecting** (Fig. 4: block selects 408 and 404) **one of said plurality of error detection and/or correction techniques/ALGORITHMS** of said electronic device based on an outcome of said comparing step (Fig. 4: block compares 407 and 402-403); determining an error rate (Fig. 4: block decision 401) corresponding to said received data, said error rate being determined by an initial one of said plurality of error detection and/or correction techniques (Fig. 4: block selects 408 and 404).

Ott also discloses a procedure wherein said error threshold value corresponds to an error rate which will ensure that said selected error detection and/or correction technique is one which consumes a lowest amount of power while maintaining a desired signal-to noise ratio in Fig. 4.

Not specifically described in detail by **Ott** is the step whereby the selected algorithm is also effected using mathematical formulation via convolutional or turbo coding along with interleaving/RLL means.

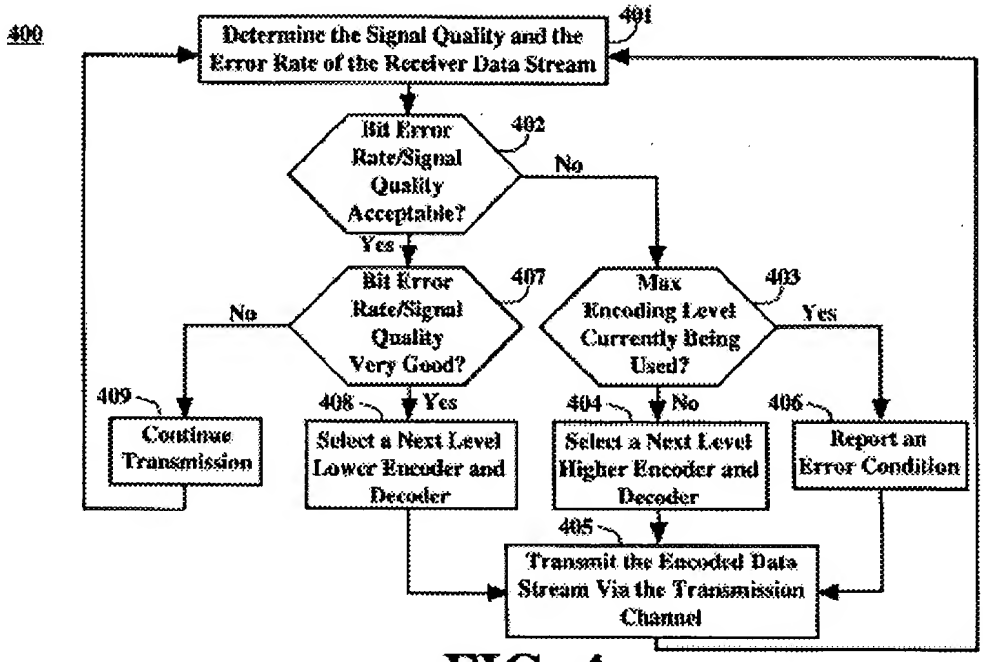


FIG. 4

However Kobayashi et al., in an analogous art, discloses algorithm means wherein such technique is performed. {See **Kobayashi**, Id., for algorithm switching means to select one ECC codec algorithm out of a plurality of encoding/decoding algorithms based on computation needs of a user at col. 4 line 30 et seq. and Figs. 1-14}. **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the process of **Ott** by including therein the technique of substituting ECC means *such as turbo/convolutional/RLL/CRC/RS codes* as disclosed by **Kobayashi** because such modification would provide the procedure of **Ott** with a method whereby *"a variety of ECC, such as turbo/convolutional/RLL/CRC/RS codes, may be implemented based on channel conditions, inter allia, so as to optimize data processing for reduction either in power consumption or hardware overhead or both."* {See **Kobayashi,** Id., e.g., col. 3 line 36.}

Conclusion

6. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 29 Jul. 2004 prompted the new ground(s) of rejection over **Hagenauer et al.** presented in this Office action. Applicant's amendment also necessitated the new ground(s) of objection presented herein. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609(B)(2)(i). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6.1 Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for all formal communications.

Hand-delivered responses should be brought to Customer Services, 220 20th Street S., Crystal Plaza II, Lobby, Room 1B03, Arlington, VA 22202.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3609.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be

obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner
2/2/05